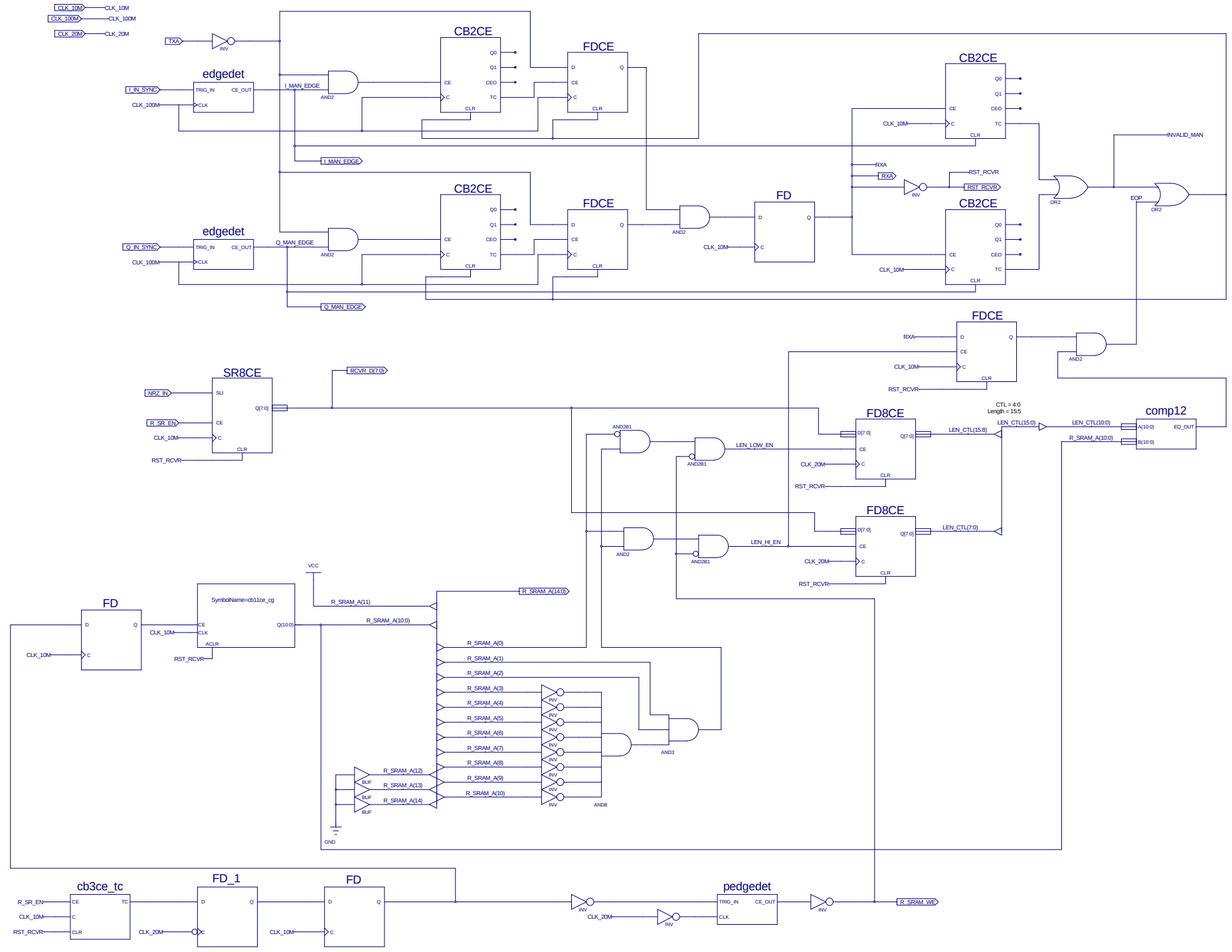
CLK_10M
CLK_100M
CLK_20M
TXA
INV
edgedet
I_IN_SYNC
TRIG_IN
CE_OUT
CLK
I_MAN_EDGE
AND2
CB2CE
Q0
Q1
CE
CEO
C
TC
CLR
FDCE
D
Q
I_MAN_EDGE
Q_IN_SYNC
Q_MAN_EDGE
FD
RXA
RST_RCVR
OR2
INVALID_MAN
EOP
SR8CE
NRZ_IN
SLI
Q[7:0]
R_SR_EN
RCVR_D[7:0]
RST_RCVR
FD8CE
AND2B1
LEN_LOW_EN
LEN_HI_EN
CTL = 4:0
Length = 15:5
LEN_CTL(15:8)
LEN_CTL(7:0)
LEN_CTL(15:0)
LEN_CTL(10:0)
R_SRAM_A(10:0)
comp12
A(10:0)
B(10:0)
EQ_OUT
VCC
SymbolName=cb11ce_cg
Q(10:0)
ACLR
R_SRAM_A(11)
R_SRAM_A(14:0)
R_SRAM_A(0)
R_SRAM_A(1)
R_SRAM_A(2)
R_SRAM_A(3)
R_SRAM_A(4)
R_SRAM_A(5)
R_SRAM_A(6)
R_SRAM_A(7)
R_SRAM_A(8)
R_SRAM_A(9)
R_SRAM_A(10)
R_SRAM_A(12)
R_SRAM_A(13)
R_SRAM_A(14)
BUF
AND3
AND8
GND
cb3ce_tc
FD_1
pedgedet
R_SRAM_WE